Chik Patrick Yue, Ph.D.
Mobile: +852 9789-5981 | eepatrick@ust.hk | http://yuegroup.ust.hk/

Education

Stanford University	Ph.D. in Electrical Engineering	1998
Stanford University	M.S. in Electrical Engineering	1994
University of Texas at Austin	B.S. in Electrical Engineering (Highest Honors)	1992

Academic Experience

Hong Kong University of Science and Technology

- Professor, ECE Department — 2011 – Present
- Director, Center for Industry Engagement and Internship, School of Engineering — 2012 – Present
- Director, HKUST-Qualcomm Joint Innovation and Research Laboratory — 2013 – Present
- Visiting Professor, ECE Department (on sabbatical from UC Santa Barbara) — 2010 – 2011

- *Research projects and major funding sources*
  - ❑ PI, HKUST-Qualcomm Joint Innovation and Research Laboratory, HK$ 4,644,342 — Sep 13 – Aug 18
  - ❑ PI, Texas Instruments Fellowship under the Microelectronics Industry Partnership Program, HK$ 280,000 — Dec 12 – Dec 15
  - ❑ Co-PI, Theme-based Research Scheme, Cost-Effective and Eco-Friendly LED System-on-a-Chip (SoC), HK$ 30,103,000 — Nov 12 – May 17
  - ❑ Co-PI, Partner State Key Lab on Advanced Displays & Optoelectronic, HK$ 13,750,000 — Jul 13 – Mar 16
  - ❑ Co-PI, Innovation Technology Fund, Guangdong-Hong Kong Integrated Circuit Design Innovation Platform, HK$ 5,000,000 — Nov 11 – Nov 14

- Teaching
  - ❑ UG course – ELEC 3400 Introduction to Integrated Circuits and Systems
  - ❑ PG course – ELEC 5280 High Frequency Circuit Design

- *Service*
  - ❑ Founded the Center for Industry Engagement & Internship in the School of Engineering
  - ❑ Established the Industrial Outreach Committee for ECE and served as the committee chair
  - ❑ Technology Transfer and Entrepreneurship
    - ✓ Technology Transfer Center Technology Review Committee member
    - ✓ Committee member of the Joint Minor Program in Entrepreneurship by SBM & SENG
    - ✓ Judge for the HKUST One Million Dollar Entrepreneurship Competition
  - ❑ Faculty Search Committee member of the HKUST-Xi'an Jiao Tong University Joint School of Sustainable Development representing SENG
  - ❑ ECE Branding Committee member
  - ❑ ECE Undergraduate Circle Committee member

University of California Santa Barbara

- Professor, ECE Department — 2010 – 2013
- Associate Director, Computer Engineering Program — 2007 – 2010
- Associate Professor (tenured), ECE Department — 2006 – 2010

Carnegie Mellon University

- Assistant Professor, ECE Department — 2003 – 2006

Stanford University

- Consulting Assistant Professor (part-time), EE Department — 2001 – 2003

Industry Experience

Non-executive Director, LEDoS Technologies Ltd., Hong Kong SAR, China	2011 – Present
Non-executive Director, BMTPow Ltd., Hong Kong SAR, China	2009 – Present
Technical Advisor, Riverwood Capital LLC, Menlo Park, CA	2011 – Present
Technical Advisor, Silicon Federation Inc., Shanghai, China	2010 – Present
Technical Advisor, Altobeam Inc., Beijing, China	2007 – Present
Technical Consultant, IC Design Group of ASTRI, Hong Kong SAR, China	2011 – 2012
Member of Technical Staff, Aèluros Inc. (acquired by Broadcom), CA	2002 – 2003
Co-founder, Atheros Communication Inc. (acquired by Qualcomm), CA	1998 – 2002

Professional Activities and Memberships

- Editor
  - IEEE Electron Devices Letter 2011 – Present
- Conference General Chair
  - International Symposium on VLSI Design, Automation and Test (VLSI-DAT) 2012, 2013
- Conference Technical Program Committee Chair
  - IEEE MTT-S International Wireless Symposium (IWS) 2014 – Present
  - IEEE International Symposium on RFIntegration Technology (RFIT) 2012
  - International Symposium on VLSI Design, Automation and Test (VLSI-DAT) 2010, 2011
- Conference Technical Program Committee Member
  - IEEE Symposium on VLSI Circuits (VLSI) 2014 – Present
  - IEEE Radio Frequency Integrated Circuits Symposium (RFIC) 2004 – Present
  - IEEE Asian Solid-State Circuits Conference (A-SSCC) 2005 – 2012
- IEEE Senior Member 2005 – Present
- IEEE Electron Device Society VLSI Technology and Circuits Committee Member 2005 – 2010

Awards and Honors

- An all-time most cited paper in *IEEE Journal of Solid-State Circuits (JSSC)* for "On-Chip Spiral Inductors with Patterned Ground Shield for Si-Based RF ICs" (Google Citation Index: 1121)
- Co-recipient of the *2003 IEEE International Solid-State Circuits Conference (ISSCC)* Jack Kilby Best Student Paper Award for "10 GHz Clock Distribution Using Coupled Standing-Wave Oscillators."

Publication Summary

- Over 90 peer-reviewed articles
- Citations: 4052, h-index: 26, i10-index: 41 (1 paper with over 1000 citation and 9 with over 100 citations)
- 2 book chapters
- 14 issued and pending U.S. Patents

Contribution to IEEE Solid-State Circuits Society Conferences and Journals

- 6 IEEE Journal of Solid-State Circuits (JSSC) papers (lead author of one of the all-time most cited paper with over 1000 citation and 4 others with over 100 citations)
- 8 IEEE International Solid-State Circuits Conference (ISSCC) papers & 1 SRP poster (co-author of the 2003 ISSCC Best Student paper)
- 9 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) papers (one invited paper in 2005)
- 4 IEEE VLSI Circuit Symposium (VLSI) papers
- 5 IEEE Custom Integrated Circuits Conference (CICC) papers
- 1 IEEE Asian Solid-State Circuits Conference (A-SSCC) paper

Current Research Projects

- High-speed (100 Gbit/s) optical communication transceiver system-on-a-chip (SoC)
- Wireless power transfer and power management IC for biomedical implants
- Multi-functional LED-on-silicon microsystems for lighting, display, and visible light communication

Most Cited Publications (with at least 100 citations)

1. C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," IEEE Journal of Solid-State Circuits, vol. 33, no. 5, pp. 743–752, May 1998. (Google Citation Index: 1121)
2. C. P. Yue and S. S. Wong, "Physical Modeling of Spiral Inductors on Silicon," *IEEE Transactions of Electron Devices*, vol. 47, no. 3, pp. 560–568, March 2000. (Google Citation Index: 595)
3. C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, "A Physical Model for Planar Spiral Inductors on Silicon," in *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 155–158, Dec. 1996. (Google Citation Index: 339)
4. M. Zargari, D. Su, C. P. Yue, S. Rabii, D. Weber, B. Kaczynski, S. Mehta, K. Singh, S. Mendis, and B. Wooley, "A 5-GHz CMOS Transceiver for IEEE 802.11a Wireless LAN," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1688–1694, December 2002. (Google Citation Index: 219)
5. T. Soorapanth, C. P. Yue, D. K. Shaeffer, T. H. Lee, and S. S. Wong, "Analysis and Optimization of Accumulation-Mode Varactor for RF ICs," in *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 32–33, June 1998. (Google Citation Index: 140)
6. D. K. Shaeffer, A. R. Shahani, S. S. Mohan, H. Samavati, H. Rategh, M. M. Hershenson, M. Xu, C. P. Yue, D. Eddleman, and T. H. Lee, "A 115-mW, 0.5-um CMOS GPS Receiver with Wide Dynamic-Range Active Filters," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2219–2231, Dec. 1998. (Google Citation Index: 123)
7. R. T. Chang, N. Talwalkar, C. P. Yue, and S. S. Wong, "Near speed-of-light signaling over on-chip electrical interconnects," *IEEE Journal of Solid-State Circuits*, no. 5, pp. 834–838, May 2003. (Google Citation Index: 115)
8. F. O'Mahony, C. P. Yue, M. A. Horowitz, and S. S. Wong, "A 10-GHz Global Clock Distribution Using Coupled Standing-Wave Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 11, pp. 1813‧1820, November 2003. (Google Citation Index: 111)
9. N. A. Talwalkar, C. P. Yue, H. Gan, and S. S. Wong, "Integrated CMOS transmit-receive switch using LC-tuned substrate bias for 2.4-GHz and 5.2-GHz applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 6, pp. 863–870, June 2004. (Google Citation Index: 103)

Book Chapters

B1 C. P. Yue, J. Park, R. Sun, L. R. Carley, and F. O'Mahony, "Low-Power, Parallel Interface with Continuous-Time Adaptive Passive Equalizer and Crosstalk Cancellation," in *Design of High-Speed Communications Circuits,* edited by Ramesh Harjani, World Scientific Publishing, ISBN: 981-256-590-6, Jan. 2006.

B2 T. H. Lee, M.M. Hershenson, S. S. Mohan, H. Samavati, and C. P. Yue, "RF Passive IC Components," in *The VLSI Handbook,* edited by Wai-Kai Chen, CRC Press and IEEE Press, ISBN: 084-938-593-8, 1999.

Patents

P1 K. M. Lau, C. Yue, Z. Liu, "LEDoS Projection System," U.S. Patent Application No. 14/054,641, filed on Oct. 15, 2013.

P2 L. Pileggi, C. P. Yue, R. S. Blanton, and T. Vogels, "System and Method to Test Integrated Circuits on a Wafer," U.S. Patent No. 7,325,180, January 29, 2008.

P3 N. Talwalkar, C. P. Yue, and S. S. Wong, "Apparatus and Method for Adjusting the Substrate Impedance of a MOS Transistor," U.S. Patent No. 7,236,044, June 26, 2007.

P4 C. P. Yue, "Integrated Balun and Transformer Structure," U.S. Patent No. 6,717,502, April 6, 2004.

P5 C. P. Yue, "Planar Inductor with Segmented Conductive Plane," U.S. Patent No. 6,593,838, July 15, 2003.

P6 C. P. Yue, S. S. Wong, D. K. Su, and W. J. McFarland, "System for Providing Electrostatic Discharge Protection for High-Speed Integrated Circuits," U.S. Patent No. 6,597,227, July 22, 2003.

P7 C. P. Yue, S. S. Wong, D. K. Su, and W. J. McFarland, "System for Providing Electrostatic Discharge Protection for High-Speed Integrated Circuits," U.S. Patent No. 6,593,794, July 15, 2003.

P8 C. P. Yue, S. S. Wong, D. K. Su, and W. J. McFarland, "System for Providing Electrostatic Discharge Protection for High-Speed Integrated Circuits," U.S. Patent No. 6,509,779 B2, January 2, 2003.

P9 C. P. Yue, M. Zargari, and D. K. Su, "RF Integrated Circuit Layout," U.S. Patent No. 6,483,188, November 19, 2002.

P10 D. K. Su, C. P. Yue, D. J. Weber, and M. Zargari, "Synthesizer with Lock Detector, Lock Algorithm, Extended Range VCO and a Simplified Dual Modulus Divider," U.S. Patent No. 6,731,176, May 4, 2004.

P11 D. K. Su, C. P. Yue, D. J. Weber, and M. Zargari, "Synthesizer with Lock Detector, Lock Algorithm, Extended Range VCO and a Simplified Dual Modulus Divider," U.S. Patent No. 6,570,453, May 27, 2003.

P12 D. K. Su, C. P. Yue, D. J. Weber, and M. Zargari, "Synthesizer with Lock Detector, Lock Algorithm, Extended Range VCO and a Simplified Dual Modulus Divider," U.S. Patent No. 6,404,289, June 11, 2002.

P13 D. J. Weber, C. P. Yue, and D. K. Su, "CMOS Transceiver Having an Integrated Power Amplifier," U.S. Patent No. 6,504,433, January 7, 2003.

P14 D. J. Weber, C. P. Yue, and D. K. Su, "CMOS Transceiver Having an Integrated Power Amplifier," U.S. Patent No. 6,504,431, January 7, 2003.

Selected Publications by Research Topics (in the last 5 years)

Power management circuits for biomedical and communication SoC

- Y. Lu, W.-H. Ki, and C. P. Yue, "A 0.65ns Response Time 3.01ps FOM Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power-Supply-Rejection for Wideband Communication Systems," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2014, accepted for publication.
- Rongxiang Wu, Wei Li, Johnny K.O. Sin, and C. Patrick Yue, "Design and Characterization of Wireless Power Links for Brain-Machine Interface Applications," accepted for publication in *IEEE Transactions on Power Electronics*, 2014.
- Y. Lu, X. Li, W.-H. Ki, C.-Y. Tsui, and C. P. Yue, "A 13.56MHz Fully Integrated 1X/2X Active Rectifier with Compensated Bias Current for Inductively Powered Devices," in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, Feb. 2013.
- S. Raju, R. Wu, M. Chan, and C. P. Yue, "Modeling of Mutual Coupling between Planar Inductors in Wireless Power Applications," accepted for publication in *IEEE Transactions on Power Electronics*, 2013.
- R. Wu, J. K. O. Sin, and C. P. Yue, "High-Q TSV-Connected Embedded Inductor for Power Applications in μH and MHz Range," *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 339–345, January 2013.
- R. Wu, S. Raju, M. Chan, J.K.O. Sin and C.P. Yue, "Silicon-Embedded Coil for High-Efficiency Wireless Power Transfer to Implantable Biomedical ICs," *IEEE Electron Devices Letters*, vol. 34, no. 1, pp. 9–11, January 2013.
- J. Cheng, L. Xia, C. Ma, Y. Lian, X. Xu, C. P. Yue, Z. Hong, P. Y. Chiang, "A Near-Threshold, Multi-Node, Wireless Body Area Sensor Network Powered by RF Energy Harvesting," in *IEEE Custom Integrated Circuits Conference (CICC) Proceedings of Technical Papers*, September 2012.
- Y. Lu, W.-H. Ki, C. P. Yue, "Input-Adaptive Dual-Output Power Management Unit for Energy Harvesting Devices," in *IEEE 55th International Midwest Symposium on Circuits & Systems (MWSCAS) Proceedings of Technical Papers*, pp. 1080–1083, Aug. 2012.
- R. Wu, S. Raju, M. Chan, J. K. O. Sin, and C. P. Yue, "Wireless Power Link Design Using Silicon-Embedded Inductors for Brain-Machine Interface," in the *Proceedings of the 8th International Symposium on VLSI Design, Automation & Test (VLSI-DAT)*, Hsinchu, Taiwan, April 2012.
- M. N. Elzeftawi, C. P. Yue and L. Theoagarajan, "Design Challenges for Sense Amplifier and Wireless Link in High-Density Neural Recording Implants," in the *Proceedings of 6th International Symposium on VLSI Design, Automation & Test (VLSI-DAT)*, Hsinchu, Taiwan, April 2010.

CMOS wireless and optical communication SoC

- Li Sun, Quan Pan, Keh-Chung Wang, and C. Patrick Yue, "A 26–28-Gb/s Full-Rate Clock and Data Recovery Circuit with Embedded Equalizer in 65-nm CMOS," accepted for publication in *IEEE Transactions on Circuits and Systems I*.
- Q. Pan, T.-J.Yeh, C. Jou, F.-L. Hsueh, H. Luong and C. P. Yue, "A Performance Study of Layout and V_t Options for Low Noise Amplifier Design in 65-nm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Digest of Papers*, June 2012.
- B. Jung and C. P. Yue, "Trends and Outlook of Wireless I/O's for Short-Range Connectivity and Beyond," *IEEE International Symposium on Radio-Frequency Integration Technology (RFIT) Proceedings of Technical Papers*, pp. 33-36, Dec. 2011.
- P. Park, L. Chen, H.-K. Yu, and C. P. Yue, "A Fully Integrated Transmitter with Embedded Antenna for On-Wafer Wireless Testing," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1456–1463, May 2010.
- P. Park, L. Chen, L. Wang, S. Long, H. K. Yu, and C. P. Yue, "On-Wafer Wireless Testing and Mismatch Monitoring Using RF Transmitters with Integrated Antennas," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Digest of Papers*, June, 2009.
- D. H. Shin, J. E. Jang, F. O'Mahony and C. P. Yue, "A 1-mW 12-Gb/s continuous-time adaptive passive equalizer in 90-nm CMOS," in *IEEE Custom Integrated Circuits Conference (CICC) Proceedings of Technical Papers*, pp. 117–120, September 2009.
- P. Park, D. H. Shin, and C. P. Yue, "High-Linearity CMOS T/R Switch Design Above 20 GHz Using Asymmetrical Topology and AC-Floating Bias," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 4, pp. 948–956, April 2009.

Device modeling and ESD protection for high-frequency analog IC's

- L. Wang, R. Ma, A. Wang, X. Wang, B. Zhao, S. X. Wang, P. Yue, Z. Shi and Y. Cheng, "A Design Technique Overview on Broadband RF ESD Protection Circuit Designs," in *IEEE 55th International Midwest Symposium on Circuits & Systems (MWSCAS) Proceedings of Technical Papers*, Aug. 2012.
- P. Park and C. P. Yue, "Modeling of triple-well isolation and the loading effects on circuits up to 50 GHz," in *IEEE Custom Integrated Circuits Conference (CICC) Proceedings of Technical Papers*, pp. 217–220, Sept 2009.